

8-bit static shift register

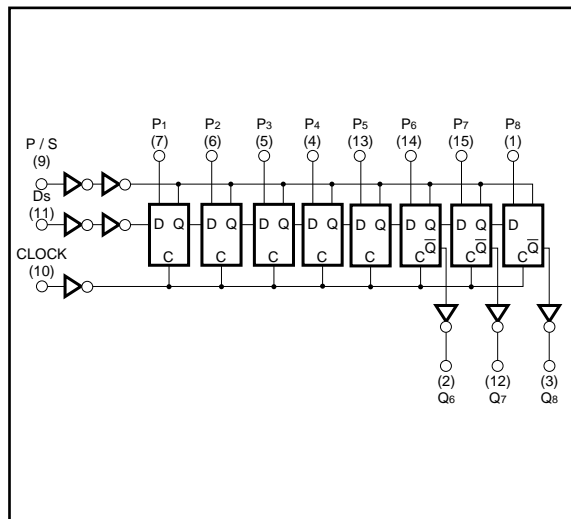
BU4021B / BU4021BF

The BU4021B and BU4021BF are 8-bit static shift registers consisting of 8 register cells, each of which has parallel input. Control of the parallel / serial control input (P / S) enables serial input / serial output with clock synchronization, as well as parallel input / serial output conversions.

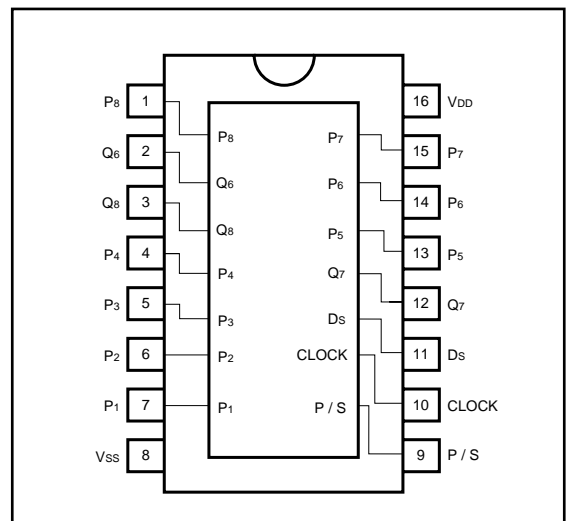
●Absolute maximum ratings ($V_{SS} = 0V$, $T_a = 25^\circ C$)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}	- 0.3 ~ + 18	V
Power dissipation	P_d	1000 (DIP), 500 (SOP)	mW
Operating temperature	T_{opr}	- 40 ~ + 85	$^\circ C$
Storage temperature	T_{stg}	- 55 ~ + 150	$^\circ C$
Input voltage	V_{IN}	- 0.3 ~ $V_{DD} + 0.3$	V

●Logic circuit diagram



●Block diagram



●Truth table

Serial operation

t	CLOCK	D_s	P / S	Q_6 ($t = n + 6$)	Q_7 ($t = n + 7$)	Q_8 ($t = n + 8$)
n	\downarrow	L	L	0	?	?
n + 1	\downarrow	H	L	1	0	?
n + 2	\downarrow	L	L	0	1	0
n + 3	\downarrow	H	L	1	0	1
	\uparrow	X	L	Q_6	Q_7	Q_8

Parallel operation

CLOCK	D_s	P / S	D_m	Q_m^*
\downarrow	X	H	L	L
\downarrow	X	H	H	H

X: Irrelevant

*: Q_6 , Q_7 , and Q_8 are external

●Electrical characteristics

DC characteristics (unless otherwise noted, $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{V}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	V _{DD} (V)	Conditions
Input high level voltage	V _{IH}	3.5	—	—	V	5	—
		7.0	—	—		10	
		11.0	—	—		15	
Input low level voltage	V _{IL}	—	—	1.5	V	5	—
		—	—	3.0		10	
		—	—	4.0		15	
Input high level current	I _{IH}	—	—	0.3	μA	15	V _{IH} = 15V
Input low level current	I _{IL}	—	—	-0.3	μA	15	V _{IL} = 0V
Output high level voltage	V _{OH}	4.95	—	—	V	5	I _O = 0mA
		9.95	—	—		10	
		14.95	—	—		15	
Output low level voltage	V _{OL}	—	—	0.05	V	5	I _O = 0mA
		—	—	0.05		10	
		—	—	0.05		15	
Output high level current	I _{OH}	-0.16	—	—	mA	5	V _{OH} = 4.6V
		-0.4	—	—		10	V _{OH} = 9.5V
		-1.2	—	—		15	V _{OH} = 13.5V
Output low level current	I _{OL}	0.44	—	—	mA	5	V _{OL} = 0.4V
		1.1	—	—		10	V _{OL} = 0.5V
		3.0	—	—		15	V _{OL} = 1.5V
Static current dissipation	I _{DD}	—	—	20	μA	5	V _I = V _{DD} , GND
		—	—	40		10	
		—	—	80		15	

Switching characteristics (unless otherwise noted, $V_{SS} = 0V$, $T_a = 25^\circ C$, $C_L = 50pF$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	V _{DD} (V)	Conditions	Measurement circuit
Output rise time	t _{TLH}	—	180	—	ns	5	—	Fig.1
		—	90	—		10		
		—	65	—		15		
Output fall time	t _{THL}	—	100	—	ns	5	—	Fig.1
		—	50	—		10		
		—	40	—		15		
"L" to "H" propagation delay time CLOCK to Q, P / S to Q	t _{PLH}	—	400	—	ns	5	—	Fig.1
		—	170	—		10		
		—	115	—		15		
"H" to "L" propagation delay time CLOCK to Q, P / S to Q	t _{PHL}	—	400	—	ns	5	—	Fig.1
		—	170	—		10		
		—	115	—		15		
Setup time	t _{su}	—	150	—	ns	5	—	Fig.1
		—	50	—		10		
		—	30	—		15		
Minimum clock pulse width	t _w (CLK)	—	150	—	ns	5	—	Fig.1
		—	75	—		10		
		—	40	—		15		
Maximum clock frequency	f (CLK) Max.	—	3.0	—	MHz	5	—	Fig.1
		—	6.0	—		10		
		—	8.0	—		15		
Maximum clock rise / fall time	t _r (CLK) t _f (CLK)	—	—	15	μs	5	—	Fig.1
	—	—	5.0	10				
	—	—	4.0	15				
Minimum P / S control pulse width	t _w (P / S)	—	150	—	ns	5	—	—
		—	75	—		10		
		—	40	—		15		
Input capacitance	C _{IN}	—	5	—	pF	—	—	—

● Measurement circuit

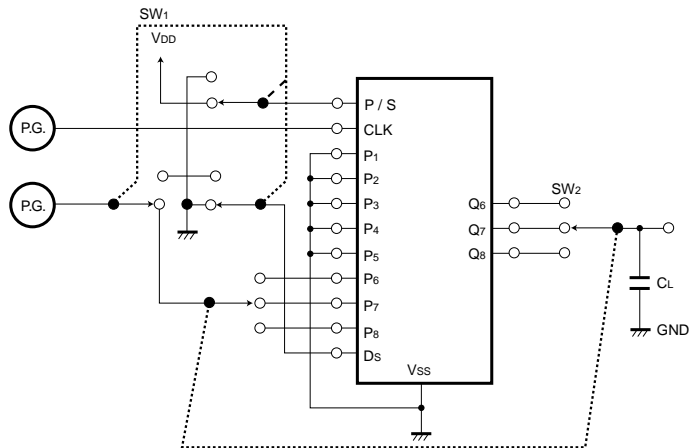


Fig.1 Switching characteristics measurement circuit

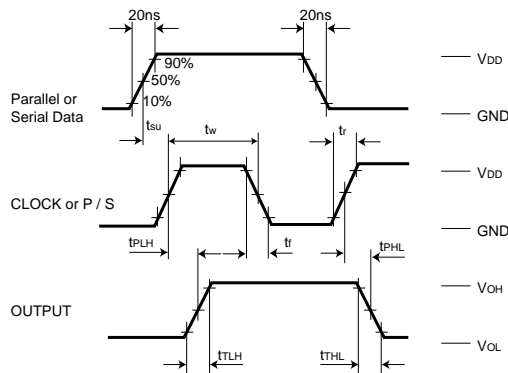


Fig.2 Switching characteristics waveform

● Electrical characteristic curve

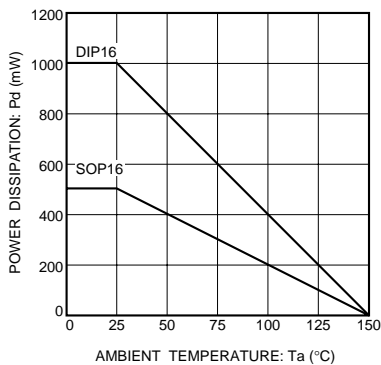


Fig.3 Power dissipation vs. ambient temperature

●External dimensions (Units: mm)

