

# TC74HC132AP, TC74HC132AF

## Quad 2-Input Schmitt NAND Gate

The TC74HC132A is a high speed CMOS 2-INPUT NAND SCHMITT TRIGGER GATE fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

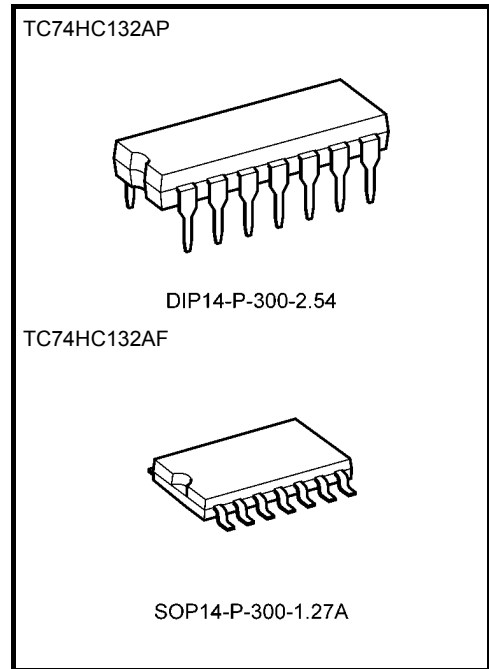
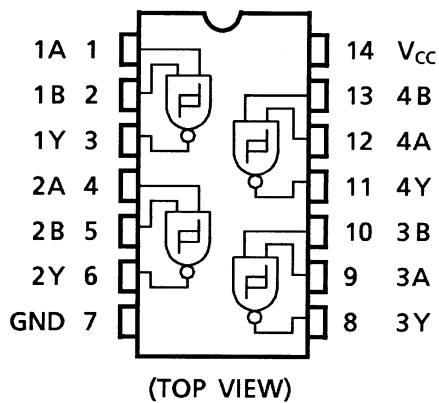
Pin configuration and function are the same as the TC74HC00A but the inputs have 25% V<sub>CC</sub> hysteresis and with its schmitt trigger inputs, the TC74HC132A can be used as a line receiver for slow input signals.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Features

- High speed:  $t_{pd} = 11 \text{ ns (typ.)}$  at  $V_{CC} = 5 \text{ V}$
- Low power dissipation:  $I_{CC} = 1 \mu\text{A (max)}$  at  $T_a = 25^\circ\text{C}$
- High noise immunity:  $V_H = 1.1 \text{ V}$  at  $V_{CC} = 5 \text{ V}$
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance:  $|I_{OH}| = I_{OL} = 4 \text{ mA (min)}$
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range:  $V_{CC} \text{ (opr)} = 2 \text{ to } 6 \text{ V}$
- Pin and function compatible with 74LS132

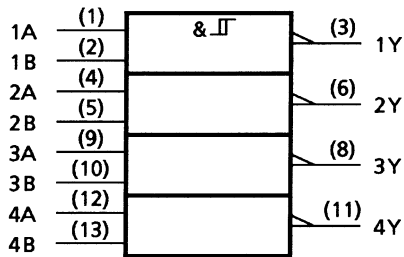
### Pin Assignment



Weight	
DIP14-P-300-2.54	: 0.96 g (typ.)
SOP14-P-300-1.27A	: 0.18 g (typ.)

Start of commercial production  
1987-11

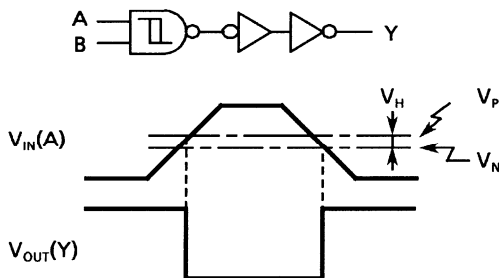
## IEC Logic Symbol



## Truth Table

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

## System Diagram, Waveform



## Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7	V
DC input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	$\pm 20$	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 50$	mA
Power dissipation	$P_D$	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}C$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of  $T_a = -40$  to  $65^{\circ}C$ . From  $T_a = 65$  to  $85^{\circ}C$  a derating factor of  $-10$  mW/ $^{\circ}C$  shall be applied until 300 mW.

## Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2 to 6	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	°C

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs must be tied to either  $V_{CC}$  or GND.

## Electrical Characteristics

### DC Characteristics

Characteristics	Symbol	Test Condition	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit		
			$V_{CC}$ (V)	Min	Typ.	Max	Min		Max	
Positive threshold voltage	$V_P$	—	2.0	1.0	1.25	1.50	1.0	1.50	V	
			4.5	2.3	2.70	3.15	2.3	3.15		
			6.0	3.0	3.50	4.20	3.0	4.20		
Negative threshold voltage	$V_N$	—	2.0	0.30	0.65	0.9	0.30	0.9	V	
			4.5	1.13	1.60	2.0	1.13	2.0		
			6.0	1.50	2.30	2.6	1.50	2.6		
Hysteresis output voltage	$V_H$	—	2.0	0.3	0.6	1.0	0.3	1.0	V	
			4.5	0.6	1.1	1.4	0.6	1.4		
			6.0	0.8	1.2	1.7	0.8	1.7		
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20 \mu\text{A}$	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
			$I_{OH} = -4 \text{ mA}$ $I_{OH} = -5.2 \text{ mA}$	4.5	4.18	4.31	—	4.13	—	
				6.0	5.68	5.80	—	5.63	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20 \mu\text{A}$	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
			$I_{OL} = 4 \text{ mA}$ $I_{OL} = 5.2 \text{ mA}$	4.5	—	0.17	0.26	—	0.33	
				6.0	—	0.18	0.26	—	0.33	
Input leakage current	$I_{IN}$	$V_{IN} = V_{CC} \text{ or } \text{GND}$	6.0	—	—	$\pm 0.1$	—	$\pm 1.0$	$\mu\text{A}$	
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC} \text{ or } \text{GND}$	6.0	—	—	1.0	—	10.0	$\mu\text{A}$	

### AC Characteristics ( $C_L = 15 \text{ pF}$ , $V_{CC} = 5 \text{ V}$ , $T_a = 25^\circ\text{C}$ , input: $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	$t_{TLH}$	—	—	4	8	ns
	$t_{THL}$					
Propagation delay time	$t_{pLH}$	—	—	11	18	ns
	$t_{pHL}$					

## AC Characteristics ( $C_L = 50 \text{ pF}$ , input: $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit
				Min	Typ.	Max	Min	Max	
Output transition time	$t_{TLH}$	—	2.0	—	30	75	—	95	ns
	$t_{THL}$		4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation delay time	$t_{pLH}$	—	2.0	—	42	110	—	140	ns
	$t_{pHL}$		4.5	—	14	22	—	28	
			6.0	—	12	19	—	24	
Input capacitance	$C_{IN}$	—	—	5	10	—	10	pF	
Power dissipation capacitance	$C_{PD}$ (Note)	—	—	29	—	—	—	pF	

Note:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per gate)}$$

## Package Dimensions

DIP14-P-300-2.54

Unit : mm

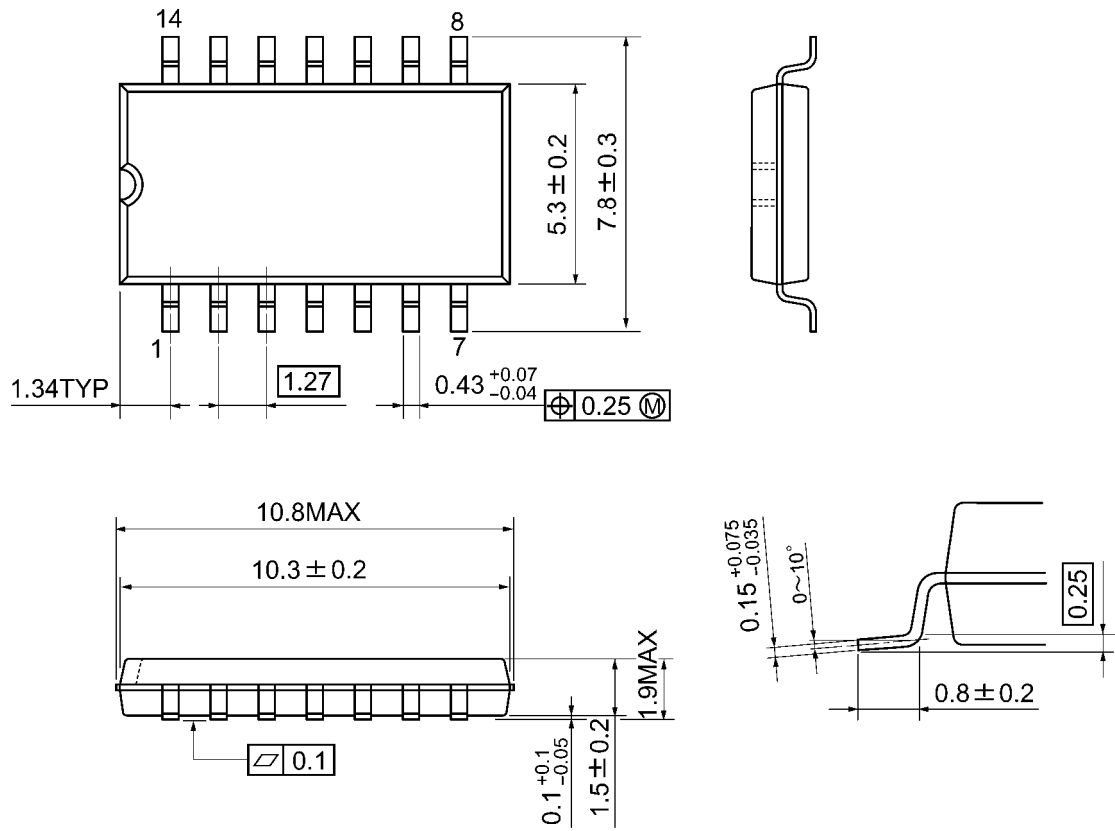


Weight: 0.96 g (typ.)

**Package Dimensions**

SOP14-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

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